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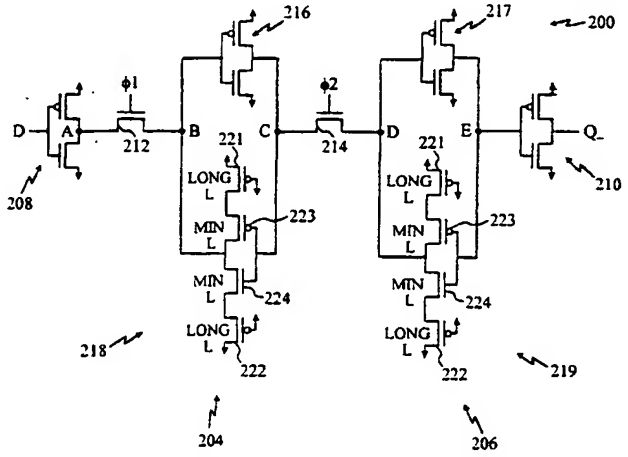
(54) Title: LOW POWER DISSIPATION MOS JAM LATCH



(57) Abstract: A feed-back inverter for use in a jam latch is disclosed. The feed-back inverter includes a first pair of NMOS and PMOS devices connected in parallel along a charge/discharge path of the inverter. A second pair of NMOS and PMOS devices are connected in parallel with the first pair but are outside of the charge/discharge path of the inverter. The first pair of devices has relatively short device lengths, whereas the second pair has relatively long device lengths. By providing devices along the charge/discharge path of the inverter that have relatively short device lengths, the capacitive load of the devices along the charge/discharge path is relatively low and the switching times are relatively short, resulting in relatively little data-power dissipation during voltage transitions. However, by providing an additional pair of complimentary devices with relatively long device lengths within the feedback inverter but outside of the charge/discharge path, the overall current drawn by the feed-back inverter is kept low in comparison with that of other inverters of the jam latch such that the other opposing, inverters dominate and permit reliable latching of data. Specific implementations are disclosed for use with two-phase and single-phase clock signals and for use within circuits having either relatively high or low voltage source levels.

WO 01/56084 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

LOW POWER DISSIPATION MOS JAM LATCH

BACKGROUND OF THE INVENTION

I. Field of the Invention

The invention generally relates to CMOS latches and in particular to a CMOS jam latch configured to dissipate relatively little power during data transitions.

II. Description of the Related Art

Fig. 1 illustrates a conventional two-phase CMOS jam latch **100** and a two-phase clock signal **102** for controlling the jam latch. The jam latch, also referred to as a full-keeper latch, operates in conjunction with the two-phase clock signal to latch, or temporarily store, a single bit of data received as an input signal D and then output the bit of data as an output signal Q. The bit of data is represented by a voltage level which is either high (VDD) or low (VSS). More specifically, during an active portion of a first phase of the clock signal (•1), the latch stores the voltage level of input signal D at an internal node C using a first pair of cross-coupled inverters **104**. During an active portion of a second phase of the clock signal (•2), the latch outputs the voltage level stored at node C as an output signal Q using the second pair of cross-coupled inverters **106**. In addition to the first and second pairs of cross-coupled inverters, the jam latch includes an input inverter **108** for initially inverting input signal D and an output inverter **110** for inverting the output of the second pair of cross-coupled inverters to yield the final output signal Q. Also, an NMOS pass gate **112**, having a gate receiving the first phase clock signal (•1), interconnects input inverter **108** and the first pair of cross-coupled inverters **104**. A second NMOS pass gate **114**, having a gate receiving the second phase clock signal (•2), interconnects the first pair of cross-coupled inverters **104** and the second pair of cross-coupled inverters **106**.

Each pair of cross-coupled inverters includes a feed forward inverter **116, 117** and a feed-back inverter **118, 119** each configured with a pair of complimentary PMOS and NMOS transistor devices. The input and output inverters also include complimentary PMOS and NMOS devices. Note that,

when clock phase •1 is active, input inverter **108** and feed-back inverter **118** of the first pair of cross-coupled inverters both attempt to assert voltage levels on nodes A and B. Likewise, when clock phase •2 is active, feed-forward inverter **116** of the first pair of cross-coupled inverters and feed-back inverter **119** of the second pair of cross-coupled inverters both attempt to assert voltage levels on nodes C and D. To ensure reliable operation, the gate lengths (L) of the PMOS and NMOS devices of feed-back inverter **118** are longer than gate lengths of the corresponding PMOS and NMOS devices of input inverter **108**. In other words, the physical distances between the source and drain components of the devices of the feed-back inverter are greater than the physical distances between the source and drain of the devices of the input inverter. As a result, when pass gate **112** closes during an active portion of clock phase •1, the devices of input inverter **108** dominate over those of feed-back inverter **118**, ensuring that the input inverter sets the voltage at nodes A and B. Hence, the current flowing through the input inverter is greater than the current flowing through the feed-back inverter, thereby allowing the devices of the input inverter to pull-up or pull-down the voltage at nodes A and B despite countervailing action of both devices of the feed-back inverter. Likewise, the gate lengths of the PMOS and NMOS devices of feed-back inverter **119** are longer than gate lengths of the PMOS and NMOS devices of feed-forward inverter **116**. As a result, when pass gate **114** closes during an active portion of clock phase •2, the devices of feed-forward inverter **116** dominate over those of feed-back inverter **119**, ensuring that the feed-forward inverter **116** sets the voltage at nodes C and D.

Although the conventional jam latch design of **FIG. 1** has been found effective for many applications, problems arise when using the latch within applications which must consume relatively little power, such as circuits for use within mobile telephones or other battery operated devices. In particular, the jam latch has relatively high data-power dissipation (also referred to as dynamic power dissipation). Data-power dissipation occurs when the voltage applied to the gates of the devices of the inverters change from one state to another. During the change, current is conducted through the devices of the inverters from VDD to VSS. Because the device length (L) of the devices of the

feed-back inverters are large to ensure reliable operation of the latch, the capacitances of the devices are also large and consequently switching of the devices of the feed-back inverters is relatively slow. Since the devices switch relatively slowly, a relatively large amount of current is conducted through the devices from high voltage to ground during voltage transitions. In addition, the large capacitances of the long-L feedback invertors translate to higher dynamic power dissipation since dynamic power dissipation is proportional to capacitance (CV^2f). If a circuit is provided with many jam latches of this configuration, the overall amount of data-power dissipation within the circuit may be significant, which is particularly undesirable for wireless telephones and the like.

Accordingly, it would be desirable to provide an improved jam-latch which has less data-power dissipation than the jam latch of **Fig. 1** yet which has relatively few components consuming relatively little circuit area and which also permits relatively high switching rates. It is to these ends that aspects of the invention are primarily directed.

SUMMARY OF THE INVENTION

An improved feed-back inverter for use in a jam latch is provided. The feed-back inverter includes a first pair of NMOS and PMOS devices connected in parallel along a charge/discharge path of the inverter. A second pair of NMOS and PMOS devices are connected between the first pair of devices and a voltage source (VDD) and ground (VSS) but are outside of the charge/discharge path of the inverter. The first pair of devices each have relatively short device lengths. The second pair of devices each have relatively long device lengths and, in particular, have device lengths longer than the lengths of devices within respective opposing inverters within the jam latch.

By providing the devices along the charge/discharge path of the inverter that have a relatively short device lengths, the switching times of the devices along the charge/discharge path are relatively short resulting in relatively low data-power dissipation. In addition, shorter device lengths in the charge/discharge path translate to lower dynamic power dissipation since smaller capacitances have

to be charged and discharged for each transition. However, by providing an additional pair of complimentary devices between VDD and VSS with relatively long device lengths positioned outside of the charge/discharge path of the inverter, the overall strength of the feed-back inverter is kept low in comparison with that of the opposing inverters of the jam latch such that the opposing inverters dominate to thereby permits reliable latching of data.

In an exemplary embodiment, the jam latch includes two pairs of cross-coupled inverters connected in series along a data path, with each pair having a feed-forward inverter and a feed-back inverter. An input inverter is connected between an input line and the first pair of cross-coupled inverters. An output inverter is connected between an output of the second pair of cross-coupled inverters and an output line. With this configuration, the input inverter is the respective opposing inverter of the first feed-back inverter. The first feed-forward inverter is the respective opposing inverter to the second feed-back inverter. The second pair of devices of the first feed-back inverter have device lengths greater than the devices of the input inverter and the input inverter dominates over the first feed-back inverter. Likewise, the second pair of devices of the second feed-back inverter have device lengths greater than devices of the first feed-forward inverter and the first feed-forward inverter dominates over the second feed-back inverter.

Specific exemplary embodiments are provided, including two-phase and single-phase jam latches for use in circuits having a relatively high VDD and two-phase and single-phase jam latches for use in circuits having a relatively low VDD. Method embodiments of the invention are also provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit schematic illustrating a conventional two-phase jam latch.

FIG. 2 is a circuit schematic illustrating a power-efficient two-phase jam latch, configured in accordance with a first exemplary embodiment of the invention, for use with a relatively high VDD.

FIG. 3 is a circuit schematic illustrating a power-efficient single-phase jam latch, configured in accordance with a second exemplary embodiment of the invention, for use with a relatively high VDD.

FIG. 4 is a circuit schematic illustrating a power-efficient two-phase jam latch, configured in accordance with a third exemplary embodiment of the invention, for use with a relatively low VDD.

FIG. 5 is a circuit schematic illustrating a power-efficient single-phase jam latch, configured in accordance with a fourth exemplary embodiment of the invention, for use with a relatively low VDD.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

With reference to the remaining Figures, preferred and exemplary embodiments of the invention will be described.

FIG. 2 illustrates a two-phase CMOS jam latch **200** for use with a relatively high VDD and also illustrates a two-phase clock signal **202** for controlling the jam latch. The jam latch operates in conjunction with the two-phase clock signal (•1 and •2) to latch a single bit of data received as an input signal D and then output the bit of data as an output signal Q. The bit of data is represented by a voltage level which is either at VDD or VSS. During an active portion of •1, the latch stores the voltage level of input signal D at an internal node C using a first pair of cross-coupled inverters **204**. During an active portion of •2, the latch outputs the voltage level stored at node C as an output signal Q using the second pair of cross-coupled inverters **206**. In addition to the first and second pairs of cross-coupled inverters, the jam latch includes an input inverter **208** for initially inverting input signal D and an output inverter **210** for inverting the output of the second pair of cross-coupled inverters to yield the final output signal Q. Also, an NMOS pass gate **212**, having a gate receiving •1, interconnects input inverter **208** and the first pair of cross-coupled inverters **204**. A second NMOS pass gate **214**, having a gate receiving •2, interconnects the first pair of cross-coupled inverters **204** and the second pair of cross-coupled inverters **206**. VDD is sufficiently high compared to VSS to permit the NMOS pass gates to operate reliably. If VDD is not sufficiently high compared to

VDD, then complimentary pass gates are instead employed as described below in connection with **FIGS. 4 and 5**.

The logical operation of the latch is summarized in TABLE I with reference to exemplary inputs signals on input line D. In the example of TABLE I, the input D has been at 0 for at least one complete clock cycle thereby providing the state as shown in the first line of the table.

INPUT (D)	NODE A	NODE B	NODE C	NODE D	NODE E	OUTPUT (Q)	CLOCK PHASE 1	CLOCK PHASE 2
0	1	1	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0
1	0	0	1	0	1	0	1	0
1	0	0	1	1	0	1	0	1

TABLE I

Each pair of cross-coupled inverters includes a feed-forward inverter **216, 217** and a feed-back inverter **218, 219**. With this arrangement, when clock phase •1 is active, input inverter **208** and feed-back inverter **218** oppose one another and both attempt to assert voltage levels on nodes A and B. Also, when clock phase •2 is active, feed-forward inverter **216** and feed-back inverter **219** oppose one another and both attempt to assert voltage levels on nodes C and D. To ensure the correct logical operation as shown above in TABLE I, the devices of feed-back inverter **218** are configured to draw less current than that of the devices of input inverter **208**, thereby allowing the devices of the input inverter to pull-up or pull-down the voltage at nodes A and B despite

countervailing action of both the devices of the feed-back inverter. Likewise, the devices of feed-back inverter **219** are configured to draw less current than that of the devices of feed-forward inverter **216** such that the that current flow through feed-forward inverter **216** is greater than current flow through feed-back inverter **219**, thereby allowing the devices of feed-forward inverter **216** to pull-up or pull-down the voltage at nodes C and D despite countervailing action of both the devices of feed-back inverter **219**. Thus the feedback inverters are configured to draw relatively low current to permit opposing inverters to dominate and thereby provide reliable latching of data. Additionally, to reduce data-power dissipation during voltage transitions, the feed-back inverters are also configured to provide reduced switching times and smaller capacitance that are charged or discharged.

The relatively low current and the relatively fast switching times of the feed-back inverters in comparison with the opposing inverters are achieved by configuring the various inverters of the jam latch as follows. Each feed-forward inverter is configured with a pair of complimentary PMOS and NMOS transistor devices of device length L. Each feed-back inverter is configured with two pairs of complimentary CMOS devices: a first, long length (>L) pair of PMOS and NMOS transistor devices, **221** and **222**, respectively and a second, short length (<L) pair of PMOS and NMOS transistor devices, **223** and **224**, respectively. The long length pairs of devices are connected outside charge-discharge paths of the respective feed-back inverters. The short (or "min") length pairs of devices are connected along the charge-discharge paths. By providing devices along the charge/discharge path of the feed-back inverters that have a relatively short device lengths, smaller capacitances and the switching times of the devices along the charge/discharge path are relatively short resulting in relatively low data-power dissipation. The specific device length can be set so that no more than a pre-determined minimal amount of power is consumed during the signal inversion. By providing the additional pair of complimentary devices with relatively long device lengths positioned outside of the charge/discharge path of the inverter, the overall impedance of the feed-back inverter is kept high in comparison with that of the opposing

inverters of the jam latch such that the opposing inverters dominate and permit reliable latching of data.

Exemplary device sizes for the various PMOS and NMOS devices of the jam latch of **FIG. 2** are as follows.

DEVICE	DEVICE SIZE
PMOS device of input inverter **208**	W = 0.68 μm; L = 0.26 μm
NMOS device of input inverter **208**	W = 0.34 μm; L = 0.26 μm
NMOS device **212**	W = 0.68 μm; L = 0.26 μm
PMOS device of feed-forward inverter **216**	W = 0.34 μm; L = 0.26 μm
NMOS device of feed-forward inverter **216**	W = 0.68 μm; L = 0.26 μm
PMOS device of feed-forward inverter **217**	W = 0.34 μm; L = 0.26 μm
NMOS device of feed-forward inverter **217**	W = 0.68 μm; L = 0.26 μm
NMOS pass-gate **214**	W = 0.68 μm; L = 0.26 μm
PMOS device **221**	W = 0.34 μm; L = 0.52 μm
PMOS device **223**	W = 0.34 μm; L = 0.26 μm
NMOS device **224**	W = 0.34 μm; L = 0.26 μm
NMOS device **222**	W = 0.34 μm; L = 1.30 μm
PMOS device **221**	W = 0.34 μm; L = 0.52 μm
PMOS device **223**	W = 0.34 μm; L = 0.26 μm
NMOS device **224**	W = 0.34 μm; L = 0.26 μm
NMOS device **222**	W = 0.34 μm; L = 1.30 μm
PMOS device of output inverter **200**	W = 1.36 μm; L = 0.26 μm
NMOS device of output inverter **210**	W = 0.68 μm; L = 0.26 μm

TABLE II

Thus, **FIG. 2** illustrates a jam latch for use with a two-phase clock signal and for use within a circuit having a relatively high VDD. As noted, the jam latch is configured to achieve relatively low data-power dissipation while still permitting fast switching rates. **FIGS. 3-5** illustrate alternative implementations of the jam latch also configured to achieve relatively low data-power dissipation. The alternative implementations operate, in general, similar to that of **FIG. 2** and only pertinent differences will be described.

FIG. 3 illustrates a jam latch **300** configured for use with a single-phase clock signal within a circuit having a relatively high VDD. A single-phase clock line is inverted (by an additional inverter not shown) and applied to a first NMOS pass-gate **312**. The single-phase clock line is also connected directly to the gate of a second NMOS pass-gate **314**. Thus, the two pass-gates receive complimentary versions of the input clock signal. The feed-back inverters are configured as described above in connection with **FIG. 2** to reduce data-power dissipation while still ensuring reliable operation.

FIG. 4 illustrates a two-phase jam latch **400** for use within a circuit having a relatively low VDD. Accordingly, rather than using NMOS pass-gates, jam latch **400** uses complimentary NMOS and PMOS pass-gates. Briefly, a first pass-gate **412** is provided with an NMOS device having a gate connected to the first phase of a clock signal (•1) and a PMOS device having a gate connected to a compliment of the first phase of the clock signal. An inverter is provided to invert the first phase of the clock signal to generate the compliment thereof, but is not specifically shown in **FIG. 4.** Additionally, a second pass-gate **414** is provided with an NMOS device having a gate connected to a second phase of the clock signal (•2) and a PMOS device having a gate connected to a compliment of the second phase of the clock signal. Again, a separate inverter provided for inverting the second phase of the clock signal is provided but is not specifically illustrated. By providing complimentary NMOS and PMOS devices within each pass-gate, reliable operation of the pass-gates is achieved despite a low VDD because the NMOS and PMOS devices, respectively, operate to fully pull down or pull up the voltages at their output nodes. **FIG. 5** illustrates a single-phase version of the jam latch of **FIG. 4**.

What has been described are various embodiments of jam latches configured, in part, to achieve relatively low data-power dissipation. The jam latches are advantageously employed within any circuit wherein power consumption must be minimized, such as circuits for use within mobile telephones and the like. However, the jam latches may alternatively be used in other circuits as well. Moreover, general principles of invention are applicable to other devices, besides jam latches. The embodiments described herein are merely illustrative of the invention and should not be construed as limiting the scope of the invention which is to be interpreted in accordance with the claims that follow.

CLAIMS

1. A feed-back inverter for use in a jam latch also having an input inverter, wherein an output of the feedback inverter and an output of the input inverter are connected to a common internal signal line, said feedback inverter comprising:

means for inverting a feedback signal along the internal signal line, said means for inverting having an inverting speed set so that no more than a pre-determined minimal amount of power is consumed during the signal inversion; and

current source means for providing electrical current to the means for inverting, said current source means providing less current to the means for inverting than an amount of current drawn by the input inverter so that the input inverter sets the signal voltage of the common internal signal line.

2. A circuit comprising:

first and second switching devices having gates connected, respectively, to first and second clock inputs;

a first pair of cross-coupled feed-forward and feed-back invertors connected between the first and second switching devices; and

a second pair of cross-coupled feed-forward and feed-back invertors connected to an output of the second switching device;

wherein each feedback inverter includes

first complimentary PMOS and NMOS devices connected in parallel along a charge/discharge path; and

second complimentary PMOS and NMOS devices connected, respectively, between the first PMOS and NMOS devices and a voltage source and a ground, outside of the charge/discharge path, with the second PMOS device having a gate connected to ground and with the second NMOS device having a gate connected to the voltage source.

3. The circuit of claim 2 further including an input inverter connected between an input line and the first switching device and an output inverter connected between an output of the second pair of cross-coupled invertors and an output line.

4. The circuit of claim 3 wherein the second PMOS and NMOS devices of the feed-back inverter of the first pair of cross-coupled inverters have device lengths shorter than device lengths of devices of the input inverter.

5. The circuit of claim 3 wherein the second PMOS and NMOS devices of the feed-back inverter of the second pair of cross-coupled inverters have device lengths shorter than device lengths of devices of the feed-forward inverter of the first pair of cross-coupled inverters.

6. The circuit of claim 2 wherein said first and second clock inputs are connected, respectively, to an first and second phases of a two-phase clock signal.

7. The circuit of claim 2 wherein said first and second clock inputs are connected, respectively, to inverted and un-inverted versions of a single-phase clock signal.

8. The circuit of claim 2

wherein the first switching device is a pass-gate having complementary gates connected, respectively, to inverted and un-inverted versions of a first phase of a two-phase clock signal; and

wherein the second switching device is a pass-gate having complementary gates connected, respectively, to inverted and un-inverted versions of a second phase of a two-phase clock signal.

9. The circuit of claim 2

wherein the first switching device is a pass-gate having complementary gates connected, respectively, to inverted and un-inverted versions of a single-phase clock signal; and

wherein the second switching device is a pass-gate having complementary gates connected, respectively, to un-inverted and inverted versions of the single-phase clock signal.

10. The circuit of claim 2 wherein

the first PMOS device has a source connected to a drain to the second PMOS device and a gate connected to an input of the feed-back inverter;

the first NMOS device has a drain connected to a drain of the first PMOS device, a source connected to the drain of the second NMOS device and a gate connected to the input of the feed-back inverter;

the second PMOS device has a source connected to the voltage source; and

the second NMOS device has a source connected to ground.

11. A feed-back inverter for use in an jam latch comprising:

a first pair of NMOS and PMOS devices connected in parallel along a charge/discharge path of the feedback inverter; and

a second pair of NMOS and PMOS devices connected between the first pair of devices and high voltage and ground, outside of the charge/discharge path of the feedback inverter;

wherein the first pair of devices have device lengths shorter than device lengths of the second pair of devices.

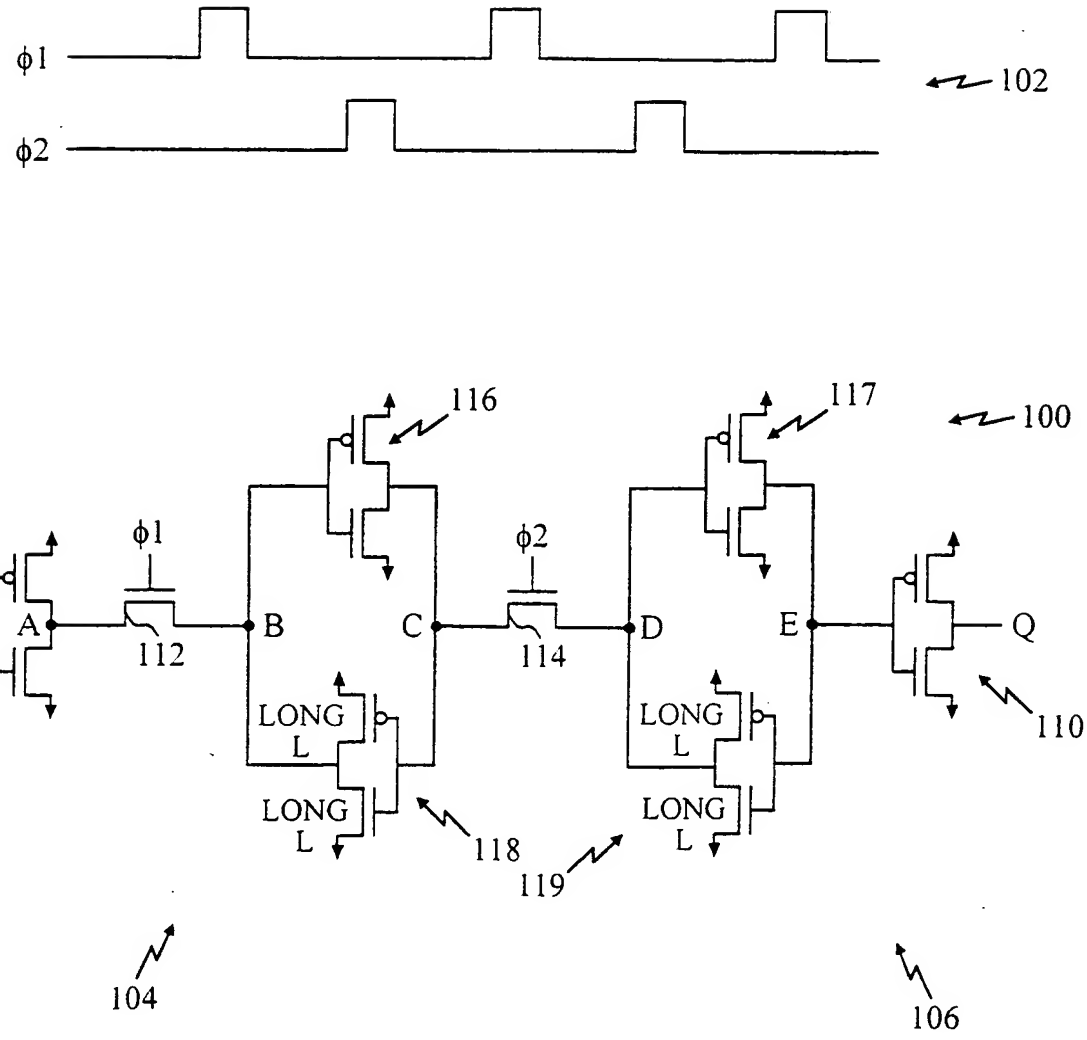
12. A method for latching an input signal comprising the steps of:

routing the signal through an input inverter, the input inverter drawing an amount of current to invert the signal;

routing the output signal of the input inverter into a feed-forward inverter; and

routing the output signal of the feed-forward inverter through a feedback inverter;

wherein an output of the feedback inverter is connected to an input of the feed-forward inverter and wherein the signal is routed within the feedback inverter through a pair of complimentary PMOS and NMOS devices while an amount electrical current is provided to the pair of devices, said amount of current provided to the pair of devices being less than the amount used by the input inverter.



(PRIOR ART)

FIG. 1

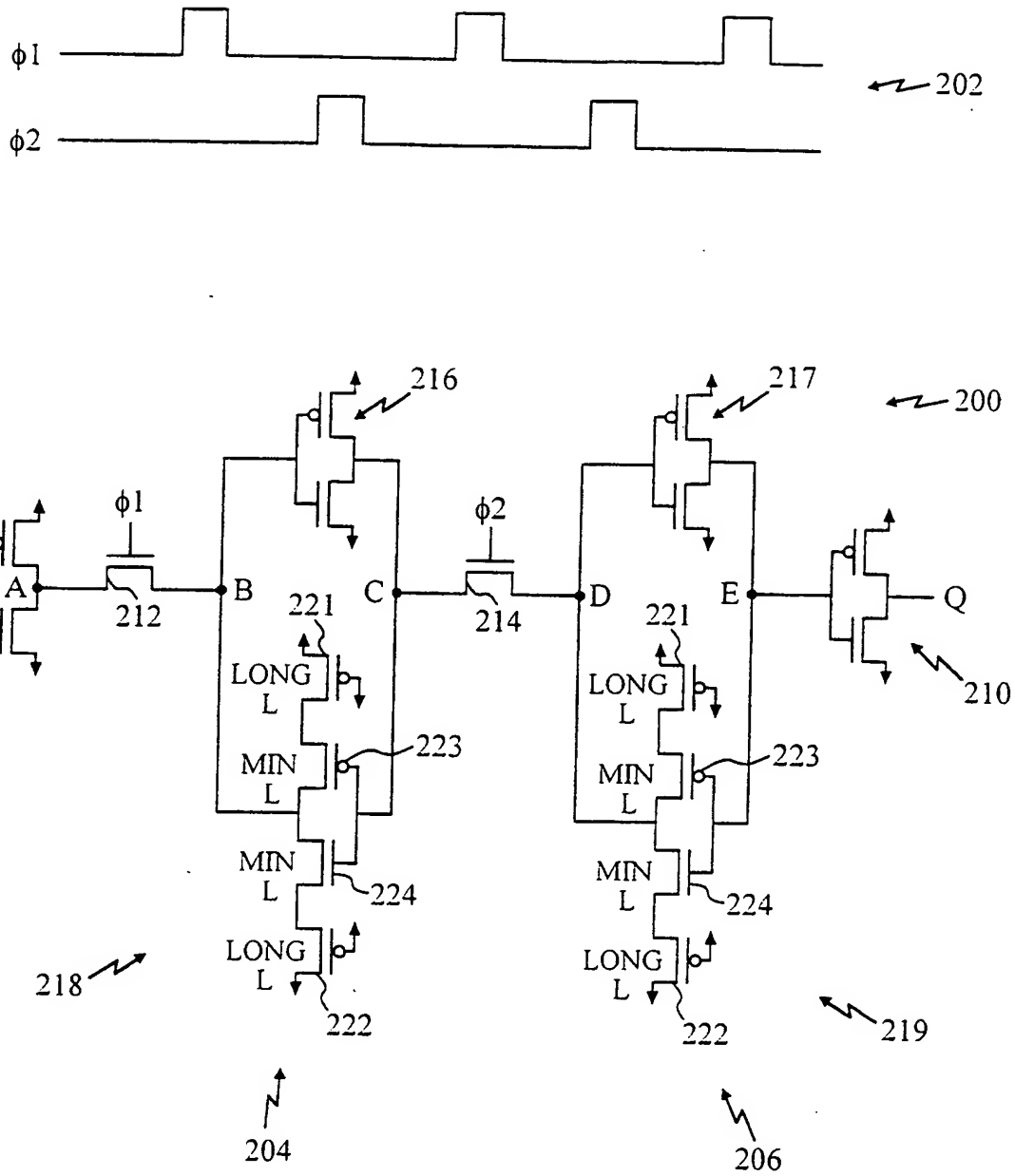


FIG. 2

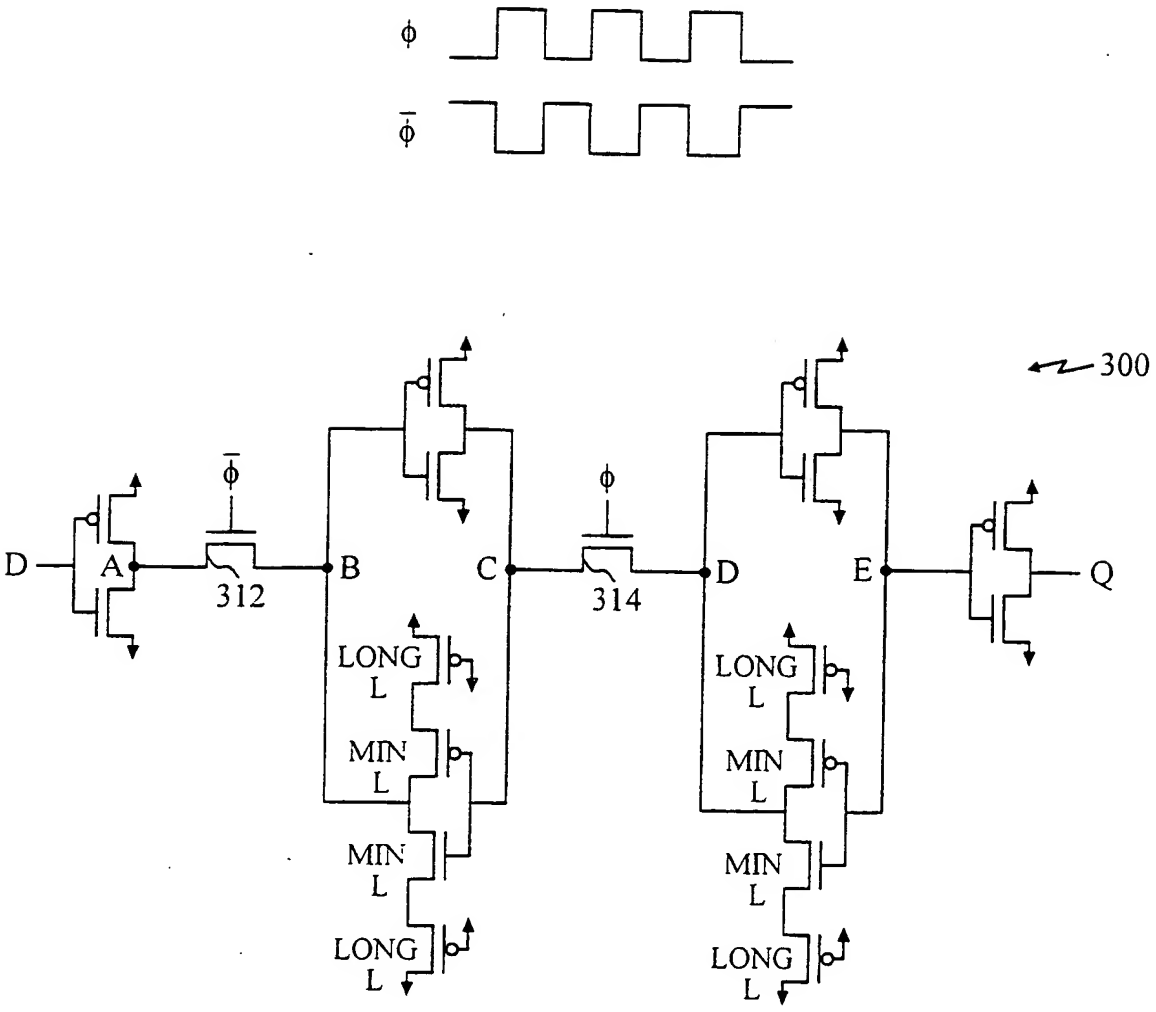
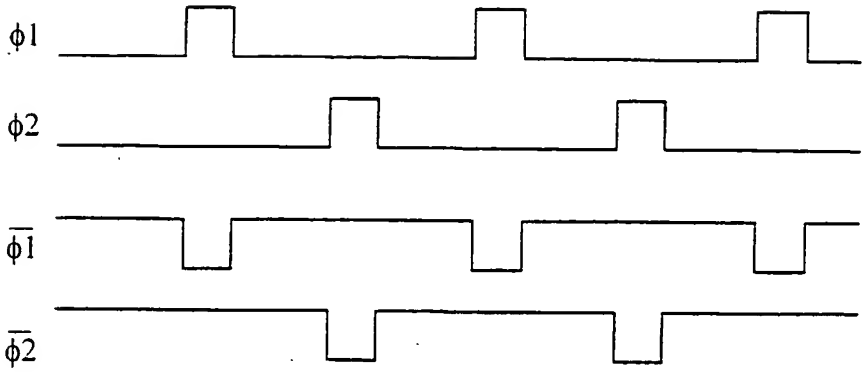


FIG. 3



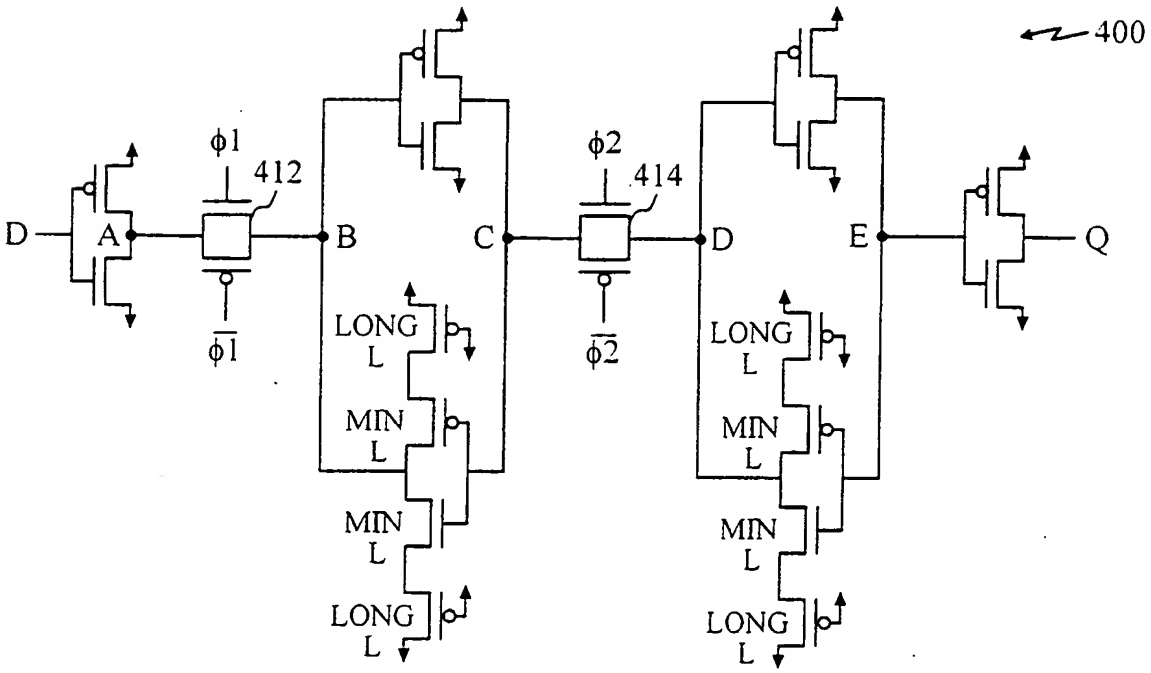


FIG. 4

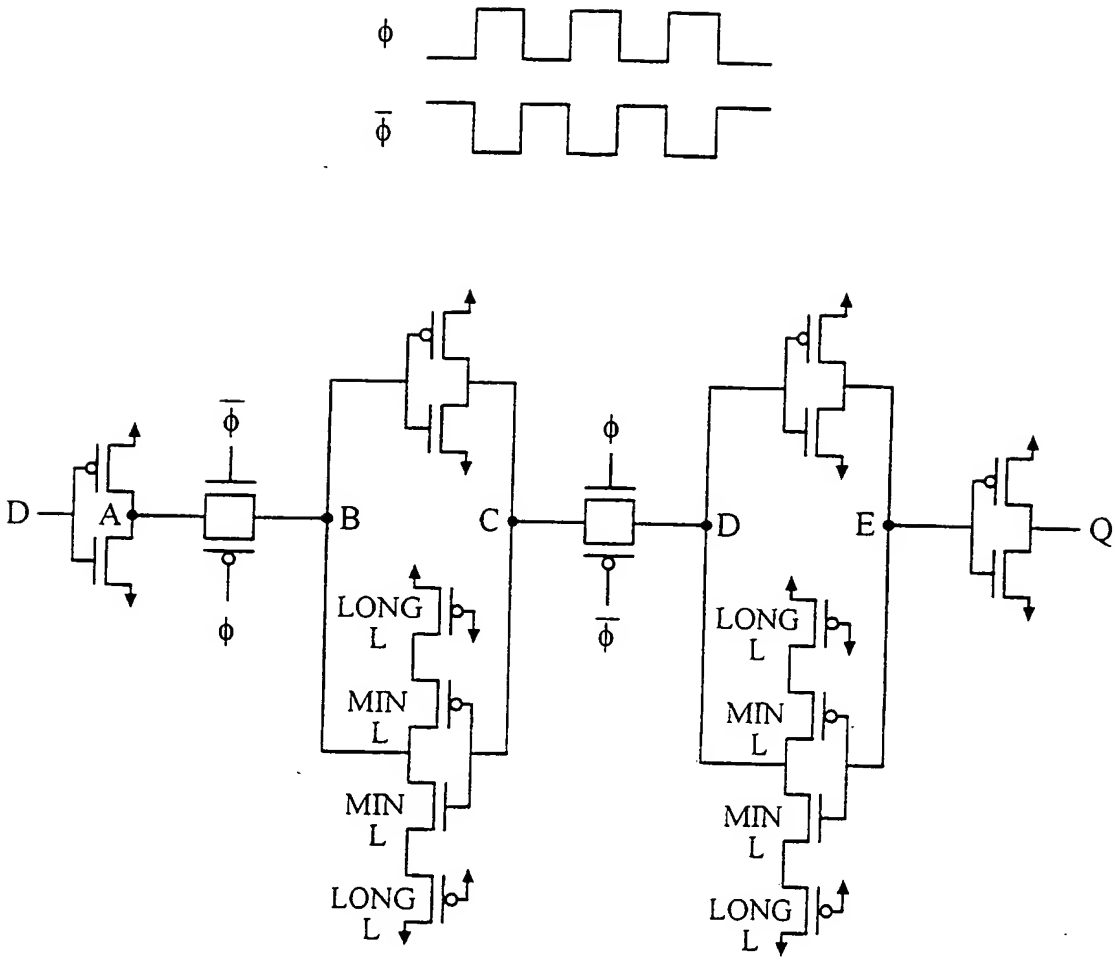


FIG. 5

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/US 01/02746

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/092 H03K19/00 H01L21/8238 H03K3/356

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ. EPO-Internal, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 567 716 A (SGS THOMSON MICROELECTRONICS) 3 November 1993 (1993-11-03) the whole document	1-12
A	US 5 170 074 A (AOKI YASUSHI) 8 December 1992 (1992-12-08) figures	6-9
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 12, 29 October 1999 (1999-10-29) & JP 11 186881 A (SHIJIE XIANJIN JITI ELECTRIC CO LTD), 9 July 1999 (1999-07-09) abstract; figures	1-12

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[X] Further documents are listed in the continuation of box C.

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INTERNATIONAL SEARCH REPORT

Inter ional Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 329 (E-452), 8 November 1986 (1986-11-08) & JP 61 134121 A (NEC CORP), 21 June 1986 (1986-06-21) abstract; figure -----	11

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US 01/02746

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